What's new in the DFM world at DAC 2006: a personal viewpoint

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Outline: DFM-related events at DAC 2006

- DFM-related Paper Sessions:
  - #5: Practical applications of DFM
  - #10: Statistical Timing Analysis
  - #43: Yield Analysis and Improvement
  - #45: Design/Technology Interaction
- DFM-related panels:
  - #26: Variation-aware analysis
  - #59: DFM, where's the Proof of Value ?
- both small and big EDA companies are announcing and/or demonstrating new DFM tools

DFM-related Paper Sessions at DAC 2006 (1/4)

- **Session #5: Practical applications of DFM**
  - 5.1 Statistical Analysis of SRAM Cell Stability:
    - Propose a (new) methodology to analyze the stability of a SRAM cell in the presence of random fluctuations
  - 5.2 Criticality Computation in Parameterized Statistical Timing:
    - A (novel) algorithm to compute the criticality probability of every edge in the timing graph
  - 5.3 Analysis of SRAM designs with Rare Failure Events:
    - A (novel) methodology for statistical SRAM design and analysis
  - 5.4 An Up-stream Design Auto-fix Flow for DFM:
    - An atomated layout modification flow for metal layers with the goal of enhancing manufaturability

DFM-related Paper Sessions at DAC 2006 (2/4)

- **Session #10: Statistical Timing Analysis**
  - 10.1 …through Learning Spatial Delay Correlations:
    - Exact modeling of spatial delay correlations is quite difficult; an experimental methodology to resolve that issue is proposed
  - 10.2 …with Correlated Non-Gaussian Parameters:
    - A scalable and efficient block-based static timing analysis, capturing spatial correlations using a grid-based model
  - 10.3 …based on Incomplete Probalistic Descriptions of Parameter Uncertainty:
    - A (new) paradigm for parameter uncertainty description
  - 10.4 Probabilistic Interval-Valued Computation:
    - A (new, improved) interval algebra that extends the classical affine form to a more rigorous statistical foundation

DFM-related Paper Sessions at DAC 2006 (3/4)

- **Session #43: Yield Analysis and Improvement**
  - 43.1 Yield Model considering Intra-Die Variations:
    - A manufacturing yield model which takes into account both layout features and manufacturing fluctuations
  - 43.2 Full Chip Gridless Routing Considering Double-Via Insertion:
    - A (new) full-chip gridless routing system considering double via insertion for yield enhancement
  - 43.3 Optimal Jumper Insertion for Antenna Avoidance:
    - An (optimal) algorithm for jumper insertion under the ratio upper-bound

DFM-related Paper Sessions at DAC 2006 (4/4)

- **Session #45: Design/Technology Interaction**
  - **45.1 Process Variation Aware OPC with Variational Lithography Modeling:**
    - **First paper to propose a true process variation-aware OPC framework: variational lithography modeling and variational edge placement.**
  - **45.2 Modeling of Intra-die Process Variations for Accurate Analysis and Optimization:**
    - **Use the Karhunen-Loève Expansion for accurate and efficient modeling of intra-die correlations**
  - **45.3 Computation of Accurate Interconnect Process Parameters:**
    - **Fast analytical model for determining accurate parasitic values for best and worst case delays under interconnect process variations**
  - **45.4 Standard Cell Characterization Considering Lithography Induced Variations:**
    - **A (new) cell characterization methodology which captures lithography induced gate length variations**

DFM-related Panel Sessions at DAC 2006 (1/2)

- **Panel #26: Variation-aware analysis**
  - William H. Joyner (IBM/SRC)
    - *Opportunity for innovation in tools and design which will move us forward over the barriers that technology has placed in our path*
  - Sani R. Nassif (IBM)
    - *New requirements for CAD, for Technology Modeling, for Device modeling, and for Technology Characterization*
  - Dennis Sylvester (Univ. Michigan)
    - *Highly regular design will be a significant help … Adaptative circuit techniques provide an alternative way of coping with large variability*
  - Vijay Pitchumani (Intel)
    - *…layout restrictions, density fill, aggressive OPC, process recipe optimization, and modeling when all else fails*
  - Clive Bittlestone (TI)
    - *Residual effects will remain components of design margin. Circuits and system techniques to support variation tolerant design and variation insensitive/corrective and adaptative design styles*
  - Norma Rodriguez (AMD)
    - *CAD industry must allow variability and yield to be understood as primary inputs to any CAD tool*
  - Riko Radojcic (Qualcomm)
    - *Addressing the systematic sources of variability through use of the new "DFM Simulators"*

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DFM-related Panel Sessions at DAC 2006 (2/2)

- **Panel #59: DFM, where's the Proof of Value ?**
  - Joe Brandenburg (Consultant)
    - *How DFM tools fit into design methodology, budget, timeline, and give examples of expected ROI*
  - Raul Camposano (Synopsys)
    - *Integrating what needs to happen in the fab with a new generation of manufacturability enabled design tools*
  - Mike Gianfagna (Aprio)
    - *All design data is verified printable and OPC correct (before tape-out)… timing and power expectations are in line with what can be manufactured*
  - Andrew Kahng (Blaze DFM)
    - *The future of DFM is in a new generation of electrically-aware DFM tools that drive power and timing requirements*
  - Naeem Zafar (Pyxis)
    - *Convergence of DFM technologies into a cohesive DFM-driven IC design flow*
  - Joe Sawicki (Mentor Graphics)
    - *Look for tools which are a natural fit into the existing design flow…*
  - Atul Sharan (Clear Shape)
    - *Move from "rule"-based to "rule+model"-based … introduction into design flows with no change… do ROI analysis on the real cost of ignoring DFM*

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What's New in EDA tools for DFM (1/2)

- Big Foundry gives access to its "fab data" through encrypted standard format. Any CAD tool can know read those previously "secret" data to implement:
  - Critical Area Analysis (and corrections)
  - Lithography Compliant Checks (and corrections)
  - CMP Checks (for parasitic extraction and dummy fill)
- EDA and Foundries+IDMs collaborate for a win-win situation: help the designer to get better chips (better yield, less power, more accurate timing) from manufacturing.
- More and more tools are DFM-aware:
  - Litho-aware routers
  - Litho-aware and CMP-aware RC extractors
  - Variability handled by Statistical approach (Timing Analysis)

What's New in EDA tools for DFM (2/2)

- Lithography Simulators, like DRC tools, are now ready for new computer architectures (multi-thread, multi-core, multi-processor)
  - Can handle bigger designs in shorter times
  - Can do incremental modifications
  - Can do more verifications
- At 90nm, Timing Closure was (is) the challenge
- At 65nm, DFM Closure is (already) the challenge